

DISPLAY ELEMENT CONTROL METHOD AND DRIVING DEVICE

Patent Number: JP2001109424

Publication date: 2001-04-20

Inventor(s): IMAMURA YOICHI

Applicant(s): SEIKO EPSON CORP

Requested Patent: JP2001109424

Application Number: JP20000257942 19910611

Priority Number(s):

IPC Classification: G09G3/20; G02F1/133; G09G3/28; G09G3/36

EC Classification:

Equivalents: JP3269501B2

Abstract

PROBLEM TO BE SOLVED: To provide a flat display device capable of preventing a display characteristic from being deteriorated due to the DC-driving or the like of a display panel caused by an abnormal signal supplied from a display controller side.

SOLUTION: Signal management controller parts 471-47n of each scanning driver LSI are cascaded, and have the same configuration. A detected signal of the controller part 471 is a data signal latch clock LP to be applied to a terminal CKB1; a detected signal of the controller part 472 is a frame start signal SP to be applied to a terminal CKB2; and a detected signal of the controller part 47n is an alternated clock FR to be applied to a terminal CKBn. The controller part 471 has a sequence processing circuit 51 comprising a signal halt detecting circuit 48 for detecting the halt of the detected signal, a signal delaying circuit 49, and a logic circuit 50. When the oscillation of the signal SP is stopped, the outputs T1-Tn of the circuit 51 are changed into a level L, and a display off signal DF (bar) becomes the level L, and a liquid crystal panel is forcibly set to a display-off mode. Since a liquid crystal impression voltage is dropped to zero even if the signal SP is stopped for some reason, DC-driving of the liquid crystal can be avoided, and the deterioration of the liquid crystal or the like can be avoided.

Data supplied from the esp@cenet database - I2